IN THE CLAIMS

Following are the claims as are currently pending for consideration:

1-3. (Canceled)

4. (Previously Presented) A computer software product including one or more recordable media having executable instructions stored thereon which, when executed by a processing device, causes the processing device to perform, at least in part, a formal verification of a circuit or other finite-state system, said executable instructions causing the processing device to:

initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configurable to express a justification property to verify by computing the symbolic simulation relation.

5. (Original) The computer software product recited in Claim 4 which, when executed by a processing device, further causes the processing device to:

compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

check the symbolic simulation relation to verify a plurality of properties expressed by a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

6-7. (Canceled)

8. (Previously Presented) A computer software product including one or more recordable media having executable instructions stored thereon which, when executed by a processing device, causes the processing device to perform, at least in part, a formal verification of a circuit or other finite-state system, said executable instructions causing the processing device to:

initialize a symbolic simulation relation for an assertion graph on a first symbolic lattice domain; and

compute the symbolic simulation relation for the assertion graph on the first symbolic lattice domain to verify the assertion graph according to a normal satisfiability criteria.

9-13. (Canceled)

14. (Previously Presented) A computer implemented method for performing, at least in part, a formal verification of a circuit or other finite-state system, said method comprising:

initializing a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configured to express a justification property to verify through computing the symbolic simulation relation.

15. (Original) The method recited in Claim 14 further comprising:

computing the symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

checking the symbolic simulation relation to verify a plurality of properties expressed by a plurality of corresponding assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

16. (Previously Presented) A computer implemented method for performing, at least in part, a formal verification of a circuit or other finite-state system, said method comprising:

specifying a justification property with an assertion graph.

17. (Original) The method recited in Claim 16 wherein the assertion graph is on a first symbolic lattice domain; and the justification property is expressed by one of a plurality of instances of the assertion graph, at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

18. (Original) The method recited in Claim 17 further comprising:

computing a symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

checking the symbolic simulation relation with a symbolic consequence labeling for the assertion graph on the first symbolic lattice domain according to a normal satisfiability criteria.

19-27. (Canceled)

28. (Previously Presented) A computer implemented verification system for performing, at least in part, a formal verification of a circuit or other finite-state system, said system comprising:

means for initializing a symbolic simulation relation for an assertion graph on a first symbolic lattice domain, wherein the assertion graph on the first symbolic lattice domain is configured to express a justification property to verify through computing the symbolic simulation relation;

means for computing the symbolic simulation relation for the assertion graph on the first symbolic lattice domain; and

means for checking the symbolic simulation relation to verify a plurality of properties expressed by a plurality of corresponding assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

29-30. (Canceled)

31. (New) The computer software product recited in Claim 4 wherein initializing the symbolic simulation relation comprises causing the processing device to:

join a Boolean predicate for an outgoing edge from an initial vertex in the assertion graph with a symbolic antecedent labeling of an edge in the assertion graph.

32. (New) The computer software product recited in Claim 31 wherein the symbolic antecedent labeling comprises a symbolic indexing function to encode a plurality of antecedent labels for a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

33. (New) The computer software product recited in Claim 8 wherein the initialized symbolic simulation relation comprises a Boolean predicate for an outgoing edge from an initial vertex in the assertion graph joined with a symbolic antecedent labeling of an edge in the assertion graph.

34. (New) The computer software product recited in Claim 33 wherein the symbolic antecedent labeling comprises a symbolic indexing function to encode a plurality of antecedent labels for a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

35. (New) The computer software product recited in Claim 34 which, when executed by a processing device, further causes the processing device to:

check the symbolic simulation relation to verify a property expressed by at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

36. (New) The computer software product recited in Claim 8 which, when executed by a processing device, further causes the processing device to:

check the symbolic simulation relation with a symbolic consequence labeling for the assertion graph on the first symbolic lattice domain according to a normal satisfiability criteria.

37. (New) The computer software product recited in Claim 36 wherein the assertion graph is on a first symbolic lattice domain; and the justification property is expressed by one of a plurality of instances of the assertion graph, at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

38. (New) The computer implemented verification system recited in Claim 28 wherein the symbolic simulation relation is initialized to comprise a Boolean predicate for an outgoing edge from an initial vertex in the assertion graph joined with a symbolic antecedent labeling of an edge in the assertion graph.

39. (New) The computer implemented verification system recited in Claim 38 wherein the symbolic antecedent labeling comprises a symbolic indexing function to encode a plurality of antecedent labels for a plurality of assertion graph instances, having at least one assertion graph instance on a second lattice domain different from the first symbolic lattice domain.

40. (New) The computer implemented verification system recited in Claim 28 wherein the symbolic simulation relation is checked with a symbolic consequence labeling for

the assertion graph on the first symbolic lattice domain according to a normal satisfiability criteria.